UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/672,367	09/28/2000	Francis X. McKeen	042390.P9578	7649

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EXAMINER
HO, THOMAS M

ART UNIT	PAPER NUMBER
2134	

DATE MAILED: 04/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *28 September 2000*.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

1.   Claims 1-22 are pending.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine

grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or

improper timewise extension of the "right to exclude" granted by a patent and to prevent possible

harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed.

Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686

F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA

1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to

overcome an actual or provisional rejection based on a nonstatutory double patenting ground

provided the conflicting application or patent is shown to be commonly owned with this

application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal

disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37

CFR 3.73(b).

Claims 1,12 are rejected under the judicially created doctrine of obviousness-type double

patenting as being unpatentable over claims 1,7, 12, 18, 23, 29, 34, 40 of U.S. Patent No.

6,633,963. Although the conflicting claims are not identical, they are not patentably distinct

from each other because the only difference between the claims is the output device of claim 1.

It would have been obvious to one of ordinary skill in the art at the time of invention to

connect an output device to the processor and memory apparatus of US Patent No. 6,633,963.

Claim Rejections - 35 USC § 102

2.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public
> use or on sale in this country, more than one year prior to the date of application for patent in the United
> States.

3.   Claims 1-17 are rejected under 35 USC 102(b) as being anticipated by Pai et al., US

Patent 5,935,247.

In reference to claim 1:

Pai et al. discloses a platform comprising:

- A processor executing in one of a normal execution mode and an isolated execution

  mode, where the processor executes the software for displaying critical data, but is

  isolated from the actual data both physically and logically. (Column 3, lines 10-40)

- A system memory including an isolated area, an isolated output area, and a non-isolated

  area, where the system memory contains the genetic code, is isolated from access by the

  processor, and the output area is the monitor, as is isolated from both processor and

  software access. (Column 2, lines 57-60)

- An output device, where the output device may either be the video card or the monitor

  display. (Column 3, line 62- Column 4, line 1)

In reference to claim 2:

Pai et al. (Column 3, line 62- Column 4, line 1) discloses the platform of claim 1 wherein the

output device is a graphics card, where the data is first given to the video card, which outputs the

data to the monitor.

In reference to claim 3:

The platform of claim 2 further comprising:

Pai et al. Figure 3 discloses a memory control hub (MCH) coupled between the system memory,

and the processor and the graphics card, the memory control hub to permit the graphics card to

access the isolated output area only when the graphics card is in isolated access mode, where the

memory control hub is the Input synchronization mode registers and the switches, which controls

and regulates the access to the isolated output area, the link between the memory and the control

hub, and permits the graphics card to access that area only when the graphics card is in isolated

mode. (Column 5, lines 20-50)

In reference to claim 4:

Pai et al. discloses the platform of claim 3 wherein the graphics card comprises:

(Column 4, lines 44-48) & (Column 5, lines 45-50) A direct memory access (DMA) controller

and wherein local storage of the data from the isolated output area is not permitted, where the

access of that stored data containing the genetic code is not permitted, and the DMA controller is

understood to be there in order to be able to access the memory(display buffer) and its video card

memory.

In reference to claim 5:

Pai et al. (Column 5, lines 5-50) discloses the platform of claim 3 wherein only the graphics card

is permitted to read the isolated output area, where the graphics card reads the isolated output

area by having the output area send the genetic code to the display buffer.

In reference to claim 6:

The platform of claim 1 further comprising:

Pai et al. (Column 4, lines 49-57) An operating system (O/S) nub having a driver to write display

data into the isolated output area when the processor is executing in isolated execution mode,

where the driver writes the display data into the isolated output area, the monitor.

In reference to claim 7:

Pai et al. (Figure 2) The platform of claim 3 further comprising:

A link between the graphics card and the MCH having an isolated transaction type, where the

MCH is the Input mode synchronization registers and the hardware switches for controlling the

isolated transactions, and the transactions it performs are isolated transactions. (Column 4, line

49 – Column 50, line 50)

In reference to claim 8:

(Column 4, lines 49-57) The platform of claim3 wherein the MCH only permits the O/S nub to write the isolated output area, where the OS nub which writes to the isolated output area is the software controlling the writing, or the video driver.

In reference to claim 9:

Pai et al. (Figure 3) The platform of claim 7 wherein the link is a secure accelerated graphics port bus, where the bus is the data line, inherently present connecting the video card with the MCH, where the line is secure since neither the processor nor the software can access the data, and where the bus is an accelerated graphics port since all video cards are graphics acceleration devices.

In reference to claim 10:

Pai et al. (Column 5, lines 40-50) discloses the platform of claim 2 wherein the graphics card comprises:

An isolated bit, where the isolated bit plane is the video buffer under the isolated execution mode where the video buffer inherently constitutes a plane of bits.

A non-isolated bit plane, where the non-isolated bit plane is the video buffer under the normal execution mode.

In reference to claim 11:

Pai et al. (Column 5, lines 40-50) discloses the platform of claim 10 wherein the graphics card

denies all external access to the isolated bit plane, where all access to isolated bit plane is

prevented.

Claim 12 is rejected for the same reasons as claim 1.

Claim 13 is rejected for the same reasons as claim 1.

In reference to claim 14:

Pai et al.(Figure 1) (Column 4, line 49 – Column 5, line 50) discloses the method of claim 13

further comprising:

(Column 5, lines 2-35) Issuing an isolated direct memory access (DMA) request for display data

in the isolated output area from a graphics card, where the isolated memory is isolated in that it

cannot be read by any other devices and the display data is located in the display buffer of the

video card, and the isolated DMA request for display data from the graphics card is read until it

is fully output to the monitor.

Refreshing the display based on the display data, where the display buffer is the memory that is

used to refresh monitor displays.

In reference to claim 15:

Pai et al. (Column 4, line 49 – Column 5, line 50) discloses the method of claim 13 wherein

preventing comprises:

- Identifying if an isolated attribute is present in a request for access to the isolated output area, where the isolated attribute is any one of the starting mechanisms that initiates the GDP, the value of the synchronization mode logic, or the value of the enable signal of the data switch device.

- Denying the request if no isolated attribute is present(Column 5, lines 19-31), where the data is never transferred if the display mode synchronization logic or the EN signal isn't set.

In reference to claim 16:

Pai et al. (Column 5, lines 40-50) discloses the method of claim 13 further comprising:

- Loading data from the isolated output area into a bit plane on a graphics card, where the bit plane is the display buffer, and the isolated output area can be the genetic code memory. (Figure 1)

- Denying all external access to the bit plane, where the access to the graphics buffer is denied to other components.

In reference to claim 17:

Pai et al. (Figure 1) discloses the method of claim 16 further comprising:

- Defining a first window for display of an image corresponding to the bit plane, where the image displayed is displayed in a first window corresponding to the bit plane or the video buffer.

- Occluding all windows but the first window, where all other windows in the display of

  figure 1 are occluded except the first window.

Claim Rejections - 35 USC § 103

4.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

5.   Claims 18-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pai et al.

In reference to claim 18:

Pai et al. (Figure 1) discloses the method of claim 13 further comprising:

- Retrieving data from the isolated output area, where the data is retrieved from the genetic

  code memory.

- Displaying an image corresponding to the data, where the image is displayed on a

  monitor.

- Pai et al. fails to explicitly disclose

- Occluding the image prior to a platform transitioning out of isolated execution mode.

It would have been obvious to one of ordinary skill in the art the occlude the image prior to transitioning out of isolated execution mode, in order to preserve the security of the information being displayed.

In reference to claim 19:

Pai et al. discloses a platform comprising:

- A processor executing in one of a normal execution mode and an isolated execution mode; (Column 3, lines 10-40) & (Column 2, lines 57-60)

- A direct memory access (DMA) controller to issue requests for access to an isolated output area; (Column 4, lines 44-48) & (Column 5, lines 45-50)

- A first interface coupled to the DMA controller to forward requests to a memory control hub (MCH); (Column 5, lines 20-50)

Pai et al. fails to disclose a second interface coupled to the DMA controller to supply output data to an output device.

The examiner takes official notice that second interfaces coupled to a DMA controller to supply output data to additional output devices was well known at the time of invention. Examples include computers that have both a video card, and a sound card, or computers with more than one video card.

It would have been obvious to one of ordinary skill in the art at the time of invention to disclose a second interface coupled to the DMA controller to supply output data to an output device, in order to allow more than one output.

In reference to claim 20:

Pai et al. discloses all of claim 20 except an interface using an AGP slot.

The examiner takes official notice that AGP interfaces were well known to those of ordinary

skill in the art at the time of invention. In fact, AGP slots were and still are the prevalent

graphics interface port in computers.

It would have been obvious to one of ordinary skill in the art at the time of invention to use an

interface that was a secure AGP slot for the video card to be attached to, because they are the

most widely used video card interface today, and would consequently be compatible with the

video cards produced by other vendors in industry.

In reference to claim 21:

Pai et al. (Column 4, line 49 – Column 5, line 50) discloses the apparatus of claim 19 wherein the

DMA controller attaches an isolated attribute to any isolated output area access request, where

the memory request is made with the initialization of the GDP, the activation of switches, and is

dependent on the current enable value of display mode synchronization logic signal.

In reference to claim 22:

Pai et al. fails to disclose the apparatus of claim 19 wherein the second interface is an audio

interface.

The examiner takes official notice that audio interfaces were well known to those of

ordinary skill in the art at the time of invention.

It would have been obvious to one of ordinary skill in the art at to time of invention to have an

audio interface coupled to the DMA controller to supply output data to an output device, to allow

audio data to be output, as opposed to simply video.

Conclusion

6.   The following prior art is made of record, but not relied upon.

*   Distributed Systems, Concepts and Designs, Coulouris et al., 1994, 2nd Edition, pgs 422-

    424 discloses a system of locks between distributed systems. These system of locks are

    well known in the art, and are sometimes called Mutex to denote of lock of mutual

    exclusion. When a processor has a lock engaged, both its memory and the processor may

    be locked or isolated. This is particularly relevant in the field of distributed systems, but

    is also well known in operating systems between concurrent processes or threads.

*

7.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Thomas M Ho whose telephone number is (703)305-8029. The

examiner can normally be reached on M-F from 8:30am – 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Gregory A. Morse can be reached at (703)308-4789. The fax phone numbers for the

organization where this application or proceeding is assigned are (703)746-7239 for regular

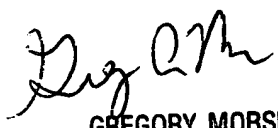communications and (703)746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)306-5484.

TMH

March 31st 2003

GREGORY MORSE
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